Interleaving ADC technique for RF-receiver architecture using FPGA.

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***Abstract —* Recent advancements in signal processing and data acquisition necessitate sampling at rates exceeding the capabilities of conventional ADC (Analog-to-Digital Converter) hardware. This paper presents a novel implementation of the interleaving ADC technique in FPGA (Field-Programmable Gate Array) hardware for super-sampling. The interleaving technique, which employs parallelism, is explored to enhance the speed and accuracy of ADCs in high-speed applications, where direct ADC sampling of signal ranging from Gigahertz to tens of Gigahertz is required. This research studies the operational theory of interleaving ADC technique and evaluating its performance advantages, operational characteristics, and inherent trade-offs. An experiment in FPGA simulation is conducted to confirm the findings of this paper.**

1. INTRODUCTION

In digital signal processing (DSP), Analog-to-Digital Converters (ADC) plays a pivotal role in translating analog signals into digital data. Conventional ADC have served as the backbone of this process, in which it quantizes continuous analog signal into a finite set of discrete digital values. This quantization process involves sampling the signal at discrete intervals of time and amplitude, effectively translating analog input series of digital numbers that represents the signals amplitude at each sampled point. This method allows ADCs integral to a myriad of applications ranging from audio and video processing to telecommunication and data acquisition.

However, the very nature of conventional ADCs introduces limitations, particularly in their sampling rate and bandwidth. The sampling rate, crucial for determining how frequently the analog signal is captured, is limited by the ADC's design and technology. This limitation becomes particularly pronounced at higher frequencies, where the need to sample more frequently to accurately capture the signal exceeds the ADC's capability. Additionally, the ADC's bandwidth, which defines the range of frequencies it can effectively convert, is intrinsically tied to its sampling rate. As the signal frequency approaches the ADC's maximum bandwidth, the accuracy of conversion decreases, impacting the fidelity of the digital output. These constraints are amplified in scenarios demanding high-frequency signal processing, where maintaining signal integrity and resolution is paramount. As the demands on digital signal processing systems have escalated, especially with the advent of applications involving ultra-high frequency signals, the speed and resolution offered by traditional ADCs have often proved insufficient. These limitations stem from the fact that each ADC can only sample at a certain maximum rate, determined by its design and the underlying technology.

To address these challenges, the interleaving ADC technique has been developed. This innovative approach employs multiple ADC modules operating in parallel, distributing the sampling load among them. This not only effectively increases the overall sampling rate but also allows for maintaining data integrity and resolution in environments where rapid signal processing is critical. By leveraging the power of parallel processing, interleaving ADCs offer a significant performance improvement over traditional ADC methods, making them increasingly relevant in fields requiring fast and accurate conversion of high-frequency analog signals, such as advanced telecommunications, high-speed data acquisition systems, and sophisticated radar and imaging technologies.

In addition, the ability of interleaving ADCs to sample at much higher rates revolutionizes ADC architectures across various applications, with the direct-sampling RF-receiver architecture serving as a prime example. This advancement is pivotal, as it allows for a significant reduction in hardware components in the analog portion of systems, simplifying overall design. Furthermore, this technique enhances flexibility in the digital domain, enabling the development of more sophisticated signal processing techniques and system designs. The transition towards a more digital-centric approach not only streamlines hardware requirements but also fosters new possibilities in system adaptability and performance optimization, particularly in high-frequency applications. This broader impact of interleaving ADCs underscores their versatility and transformative potential in modern digital signal processing.

1. Theory of Operation
2. *Architecture Overview.*

Interleaving ADC is a technique that applies the principle of parallelism to the task of sampling. This technique divides the sampling task among multiple ADC modules, where each module samples a distinct portion of the signal. These individual samples are then combined to form a comprehensive digital representation of the entire signal. This parallel operation not only allows for a sampling rate that is several times higher than what a single ADC module could achieve, but it also enhances the overall resolution of the ADC process. By distributing the workload across multiple modules, interleaving ADCs effectively mitigate the speed and resolution constraints faced by conventional single-module ADC systems, leading to more efficient and accurate signal digitization, especially in high-speed applications.

1. *Sampling, Quantization. Interleaving technique.*

In interleaving ADC systems, the processes of sampling and quantization are intricately intertwined and are key to the system's efficacy. Sampling, the first step in the ADC process, involves capturing the analog signal at discrete time intervals. In an interleaving ADC setup, this process is divided among multiple ADC modules, with each module sampling the signal at a different phase of the sampling clock. This staggered approach ensures that collectively, the modules cover a wider range of the signal more frequently than a single ADC could, effectively increasing the system's overall sampling rate.

Once the analog signal is sampled, it undergoes quantization, a critical process where these sampled analog values are converted into digital numbers. Each ADC module independently quantizes its sampled portion of the signal. This conversion is based on the module's resolution, which dictates how many discrete values the analog signal can be mapped to. The higher the resolution, the more accurate the representation of the analog signal in digital form. However, increased resolution also means more complex and resource-intensive quantization.

Interleaving technique refers to the process of combining the outputs of these individual ADC modules into a cohesive digital signal. This is a nuanced technique that involves aligning and merging the discretely quantized values from each module to form a unified and accurate representation of the original analog signal. This combination process must account for the timing (phase) differences between the modules. Precision in this step is critical; even slight misalignments can introduce phase errors or time skews, leading to inaccuracies in the combined digital output.

To ensure accurate combination, sophisticated alignment techniques are employed. These techniques involve adjusting the timing of each ADC module's output so that they align perfectly in time. This may include correcting for phase shifts introduced by the different paths the signal takes through each module or compensating for any inherent delays in the modules themselves. The objective is to synchronize the digital outputs in such a way that when they are combined, they form a seamless and accurate representation of the full bandwidth of the analog signal.

The final combined digital output is, therefore, a high-resolution, high-speed representation of the analog input, achieved through the parallel operation of multiple ADC modules. This output reflects not just the increased sampling rate and resolution capabilities of the interleaving ADC system but also the precision and complexity involved in the sampling, quantization, and combining processes.



Fig. 1. ADC Interleaving Architecture.

1. *Interleaving ADC spurs.*

In interleaving ADC systems, a notable disadvantage often encountered in practice is the occurrence of interleaving spurs. These spurs are undesirable spectral components that arise as a result of mismatches in timing, gain, and phase among the individual ADC modules. Ideally, if each ADC module were perfectly synchronized and identical in characteristics, these spurs would not occur. However, in real-world applications, achieving such perfection in combining multiple ADCs is extremely challenging.

The presence of interleaving ADC spurs is often an unavoidable result of the practical limitations and variances in ADC module manufacturing and operation. Even with precision engineering, differences between modules in terms of their timing accuracy, gain levels, and phase response can contribute to the formation of these spurs. For example, Texas Instrument conducts an experiment to observe the output spur of 1% phase error compared to the correct phase alignment, shown in Figure 2.

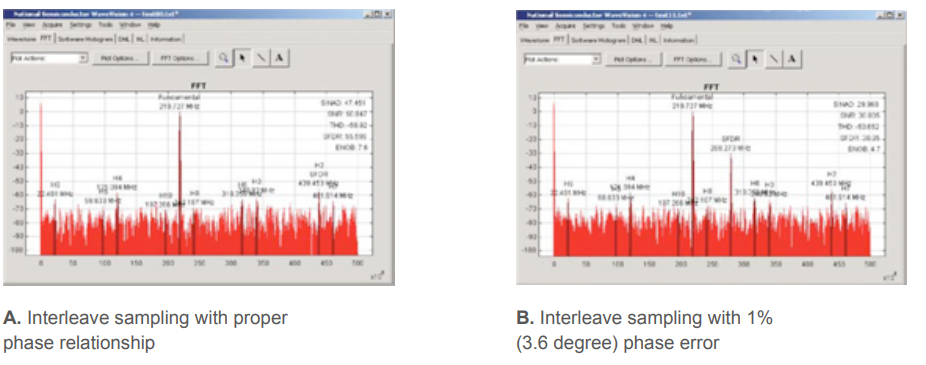


Fig. 2. ADC Interleaving phase error [1].

Fortunately, these spurs are typically deterministic, meaning they follow predictable patterns based on the ADC system’s configurations and operational parameters. This predictability allows for their mitigation in subsequent processing stages. Advanced digital signal processing (DSP) techniques can be employed to identify and filter out these spurs, improving the fidelity of the digitized signal. Techniques include digital filtering to exclude spur frequencies and calibration algorithms to adjust for mismatches in the ADC modules. While completely eliminating these spurs can be challenging, such mitigation strategies significantly reduce their impact, enhancing overall signal quality. For example, a time-interleaved ADC (TI-ADC) calibration technique introduces an algorithm to calibrate the mismatches in sampling time, gain, and phase offset among the input modules, allowing correct data alignment for the interleaving process [2].

Therefore, managing and mitigating these spurs is a critical aspect of designing and operating interleaving ADC systems, particularly in applications where signal fidelity is paramount.

1. *Implementation Complexity and Resource Utilization.*

Implementing interleaving ADC systems involves significant complexity, primarily due to the need for precise coordination among multiple ADC modules. Each module must be accurately synchronized with the others, particularly in terms of timing and phase alignment, to ensure the integrity of the combined digital output. This synchronization is essential to prevent mismatches that could lead to errors.

Such precision often requires advanced control systems capable of making real-time adjustments. Additionally, environmental factors like temperature and voltage variations can impact the performance of individual modules, further complicating the synchronization process. Therefore, interleaving ADC systems not only require careful initial design but also ongoing management to ensure they continue to perform optimally.

Another trade-off in using interleaving ADCs is the increased resource utilization. The architecture of these systems demands multiple ADC modules, each of which consumes power and requires physical space. This can lead to higher overall power consumption compared to single-module ADC systems, which is a critical factor in battery-powered or energy-sensitive applications. Furthermore, the additional processing power required for managing and combining the outputs of multiple ADC modules can result in a need for more powerful, and often more expensive, processing hardware. These factors contribute to a larger physical footprint and increased material costs, making system integration and cost management more challenging.

While these trade-offs – implementation complexity and resource utilization – pose challenges, they are often offset by the significant benefits of interleaving ADCs, such as higher sampling rates and improved resolution. These advantages are particularly valuable in applications where capturing high-frequency signals with great accuracy is paramount. As such, the decision to use interleaving ADC technology is often a balance between these trade-offs and the specific requirements of the application at hand.

1. EXPERIMENT

This research presents an experiment focused on implementing and exploring the characteristics of the interleaving ADC technique. The experiment involves developing an algorithm to synchronize four conventional ADCs, each sampling at a designated ADC\_dice rate. These ADCs are aligned using an interleaving algorithm that ensures correct timing (phase) alignment. The outcome is a combined output that effectively quadruples the rate and resolution of a single ADC, demonstrating the efficacy of the interleaving\_adc approach.

The implementation is written in Verilog, a hardware description language, with the aim of deploying it on an FPGA – hardware platform that is widely used for ADC interleaving techniques to attain high sample rate outputs. Given the project's scope and the unavailability of FPGA hardware, all functionality tests and analyses were performed in the Vivado simulation environment.

This section outlines the experimental procedure. We developed a testbench to assess the performance of the interleaving ADC technique. This testbench emulates an FPGA hardware operating at clock frequency. It processes an analog cosine input signal, which is sampled by four separate ADCs. Each ADC samples at a rate of , with a deliberate time offset between them. The testbench applies the interleaving ADC technique, merging the outputs of the four ADCs to effectively quadruple their individual sample rate and resolution. The results of the simulation are intended to validate the experiment's findings. Figure 3 shows the flowchart of the implemented interleaving technique.



Fig. 3. Interleaving ADC flowchart.

1. RESULT AND ANALYSIS

Figure X shows the simulation results. The first green waveform represents the 100MHz FPGA system clock. The orange waveform is the input analog signal. The blue waveforms depict output signals, comprising four distinct ADC samples at a lower rate with time offsets, and the combined output of the interleaved ADC with enhanced rate and resolution. Analysis confirms that the four ADCs sample at and the interleaved ADC samples at . This results in the interleaved output achieving the anticipated combined rate and resolution.

A screenshot of a computer

Description automatically generated

Fig. 4. Interleaving ADC simulation results.

Although the interleaving technique achieves a higher sample rate and resolution, it is observed that the algorithm necessitates a brief setup time before it starts producing interleaved data. Additionally, it's important to note that the evaluation was conducted in a simulation environment, where most parameters and the algorithm were ideal and deterministic, resulting in no noise or spurious signals being produced. For instance, in the simulation, the ADC dice are generated using the same clock source, which simplifies their alignment. However, in practical hardware applications, this scenario may present challenges. Each ADC might not sample precisely at 25MHz, leading to synchronization issues. This discrepancy could necessitate a more complex approach to effectively synchronize the ADC dices.

1. CONCLUSION

In conclusion, the experimental results agree with the theory of operation. Specifically, the experiment successfully implements the interleaving ADC technique, which enhances performance by combining multiple ADC instances. However, it's important to note that the simulation did not account for potential negative aspects, such as ADC spurs resulting from misalignment, or the complexity involved in addressing these issues. This research lays the groundwork in this engineering domain, presenting opportunities for further in-depth exploration. Future studies could delve into examining the characteristics of the interleaving ADC technique on actual FPGA hardware. Additionally, more intricate scenarios, such as super-sampling where the interleaving ADC produces more samples than the FPGA hardware can manage, could be investigated. Such advancements pave the way towards cutting-edge technology applicable in advanced real-world applications.

References

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